REMARKS

An Information Disclosure Statement was filed with the application on July 1, 2003 (copy attached). However, the Examiner has not indicated consideration of the references cited in the Information Disclosure Statement. It is respectfully requested that the Examiner place his initials by the listed references on form PTO-1449 submitted with the Information Disclosure Statement of July 1, 2003.

In the Office Action dated February 10, 2005, claims 1-5 and 14 were rejected under 35 U.S.C. § 102 over U.S. Patent No. 6,314,014 (Lowrey); claim 9 was rejected under § 103 over Lowrey in view of U.S. Patent No. 6,114,719 (Dill); and claims 10-13 were rejected under § 103 over Lowrey in view of U.S. Patent Application Publication No. 2003/0122170 (Apodaca).

Applicant acknowledges the indication that claims 6-8 were objected to, but would be allowable if rewritten in independent form.

Applicant has amended claims 6-8 into independent form, with the scope of each of the claims *broadened* by replacing "on" with "over" at line 3 of each of claims 6-8, and by deleting "over" at line 4 of each of claims 6-8. Claims 6-8 are in condition for allowance.

Withdrawn claims 15-22 have been cancelled, without prejudice, in favor of submission in a divisional application.

To address the suggestions made by the Office Action regarding the priority claim and the title, the priority claim and title have been amended on page 1 of the application.

Amended claim 1 now recites forming non-volatile memory cells, each formed by connecting a memory component between an electrically conductive row and an electrically conductive column, wherein the non-volatile memory cells are formed *without transistors* for reduced space usage on the semiconductor substrate by each memory cell. This subject matter is contradicted by the figures of Lowrey, which show the use of isolation transistors Q1 in each of the memory cells 120, 130, 140 depicted in Figs. 2A-2D, 3, 4, and 6A-6C. The use of transistors, as taught by Lowrey, in each memory cell is wasteful of space in a memory device. As Lowrey does not disclose the subject matter recited in claim 1, it is respectfully submitted that Lowrey does not anticipate claim 1.

Claim 2 has been amended from dependent form to independent form. Claim 2 recites that the memory components of the non-volatile memory cells are formed to have *varying*

resistance values based on at least one of: (1) varying thicknesses of electrically resistive materials that are part of respective memory components; (2) varying areas of electrically resistive materials that are part of respective memory components; and (3) varying geometric shapes of electrically resistive materials that are part of respective memory components.

In the rejection of claim 2, the Office Action referred to a passage in column 1 of Lowrey as teaching previous claim 2. Note, however, that the column 1 passage of Lowrey indicated by the Office Action refers to changes made to phase-change materials that can be programmed between a completely amorphous state and a completely crystalline state. Lowrey, 1:33-36. The changes that can be made to the phase-change materials include "changes of local order" or "changes in volume of two or more materials having different local order so as to provide a 'gray scale' represented by a multiplicity of conditions of local order spanning the spectrum between the completely amorphous and the completely crystalline states." Lowrey, 1:40-44. Although reference is made to "changes in volume" in column 1 of Lowrey, this change in volume does not refer to changing thicknesses or areas or geometric shapes of electrically resistive materials. What is referred to in the column 1 passage of Lowrey, and everywhere else in Lowrey, is changing the phase of phase-change materials to achieve different electrical characteristics. Thus, it is respectfully submitted claim 2 is not anticipated by Lowrey.

Newly added independent claim 23 recites a method of providing memory cells having respective resistive components, the resistive components connected between respective row and column traces without connecting through isolation circuitry, and where an individual one of the resistive components has a resistance value representing plural logical bits. As noted above, Lowrey requires the use of transistors as isolation circuitry between a row line and a column line. Claim 23 recites the opposite, stating that a resistive component of a memory cell is connected between respective row and column traces without connecting through isolation circuitry. Therefore, Lowrey does not teach the subject matter of claim 23.

Dependent claims, including newly added dependent claims 24-30, are allowable for at least the same reasons as corresponding independent claims. Newly added dependent claims 24-29 depend from claim 23, and newly added dependent claim 30 depends from claim 1.

In view of the allowability of base claim 1 over Lowrey, it is respectfully submitted that the obviousness rejections of claims 9-13 over Lowrey and Dill or Apodaca have also been overcome.

Allowance of all claims is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account No. 08-2025 (10010715-3).

Respectfully submitted,

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